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Applicant: Thin Film Electronics ASA
P.O.Box 1872 Vika
N-0124 OSLO NORWAY

Inventor(s): Göran Gustafsson
Trumslagaregatan 3
S-582 16 LINKÖPING SWEDEN

Peter Dyreklev
Skogsfridgatan 17
S-582 46 LINKÖPING SWEDEN

Johan Carlsson
Ekholmsvägen 219
S-589 29 LINKÖPING SWEDEN

Title of the invention: Interlayer connections for layered electronic devices

Interlayer connections for layered electronic devices

The present invention concerns interlayer connections for layered electronic devices according to the introduction of claim 1.

In multilayered electronic devices where each layer comprises a large number of conductive parts or electrodes that shall be connected to a peripheral circuitry, e.g. in an underlying substrate connections are formed by metallic vias. This will be the case of a thin-film matrix-addressable memory with e.g. a ferroelectric polymer as the memory material. It is desired that vias should have a minimal feature size, while at the same time also a high-quality metal field and step coverage is required. The use of high aspect ratio vias based on tungsten plugs has been attempted, but this requires a high temperature process that is not compatible with the melting temperatures e.g. of polymeric materials and there will hence be unsuited in that case. An alternative is to apply fan-out conducting paths on the outside of the device such that the area for each via is increased and the aspect ratio kept low. Then low-ohmic vias can be found without resorting to any metal plugs and there will only be metal-to-metal contact. The problem with this solution is that the use of fan-out conducting paths is very real-estate consuming as the area occupied by fan-out conducting paths scales as $(vs)^2$ where v increased via edge length and s the nominal edge length of an electrode matrix. A doubling of the via size results in the area of occupied by the fan-out vias becomes three times larger than the original array size.

The use of so-called staggered vias is an alternative solution as it does not consume much real estate, but it requires a number of extra (dummy) lines proportional to the inverse of the stagger depth.

The object of the present invention is to provide vias which provide a very small aspect ratio with a very low aspect ratio in one dimension and good step coverage over at least two side walls perpendicular to the conductor entering the via.

It is also an object of the invention to avoid complexity of the interconnect layout and a reduced die size of the interconnect area as compared with the e.g. fan-out solution as proposed in prior art.

These objects as well as further features and advantages are achieved according to the invention with an interconnection characterized by the features of the characterizing portion of independent claim 1.

Further features and advantages of the present invention are disclosed by the appended dependent claims.

The invention shall be better understood from the following discussion of preferred embodiments read in conjunction with the drawing figures, of which

fig. 1 shows how fan-out is used for increasing the size of vias as known in the art and mentioned above,
fig. 2 shows a rectangular via opening through an insulating interlayer, with low aspect ratio in one direction (y) and high aspect ratio in the transverse direction (x),
fig. 3 shows a side view section in the y direction through the filled via connection
fig. 4 shows a top view of four parallel stripe electrodes connecting to another layer through aligned vias according to present invention, and
fig. 5 shows a perspective view of an alternative via opening to that shown in fig. 2, now with the end walls on the short dimension tapering outwards at the top

Now follows a discussion of preferred embodiments of the present invention. A first preferred embodiment of an interlayer connection or through-layer via is illustrated in figs. 2, 3 and 4. In figs. 4 four stripe electrodes forming part of a dense array of parallel stripe electrodes are connected to separate elements of a matrix device on the left. Each stripe electrode is to be individually connected electrically through an insulating interlayer to a set of densely arrayed connecting pads, typically in the form of stripe electrodes, below the interlayer. This is achieved according to the present invention by using rectangular via connections extending parallel to the stripe electrodes as illustrated in figs. 1, 2 and 3. Due to the extended dimension in the y direction, adequate filling of the via openings with conducting material is possible, despite very small stripe electrode width.

A second preferred embodiment is illustrated in fig. 4. Here, the end walls are tapered outwards towards the top. This facilitates filling of the via

opening with conducting material and reduces the risk of "dry spots" on the contact areas against the electrode connections in the lower layer. Since the taper is in the long direction of the via opening, this does not compromise the side-by-side electrode density that can be achieved within a given design rule.

The interlayer connections according to the present invention not only permits a better exploitation of the device real estate, but also due their geometry which serves to provide a much improved aspect ratio in one dimension, i.e. the ratio $\frac{H}{Y}$ becomes low, thus ensuring a much better fill of via metal and improved contact properties in layered electronic devices. Particularly this is desirable in case of thin-film devices such as matrix-addressable memories.

CLAIMS

1. Interlayer connections for a layered electronic device particularly for storing or processing of data, wherein the device comprises electrical connections between circuitry located in two or more layers separated by interlayers of electrically insulating material, wherein electrical interlayer connections consisting of plugs or wires of highly electrically conducting material penetrate said interlayers of electrically insulating material, and wherein the interlayer connections are
characterized in that said plugs or wires have a cross section in the plane of said interlayers with dimensions that are much longer in one direction, the long dimension of representative magnitude Y, as compared to the transverse direction, the short dimension of representative magnitude X.

2. Interlayer connections according to claim 1,
characterized in that said plug or wire connects one or more narrow stripe electrodes, and that the cross section of said plug or wire has its long dimension parallel to the length-wise direction of said stripe electrode or electrodes.

3. Interlayer connections according to claim 1,
characterized in that said plug or wire is completely contained within the footprint of one of said stripe electrodes.

4. Interlayer connections according to claim 1,
characterized in that said plug or wire has a ratio between the long and short dimension $Y/X \geq 2.5$.

5. Interlayer connections according to claim 1,
characterized in that said plug or wire is formed in the same application step for said conducting material as the top surface electrode.

6. Interlayer connections according to claim 1,
characterized in that said plug or wire is formed with the end sides along the short dimension tapering outwards at the top.

ABSTRACT

Connections with an improved geometry and occupying much less real-estate compared with previous solutions are provided for layered electronic devices comprising electrical connections between circuitry located in two or more layers separated by interlayers of electrically insulating material. The interlayer connections are formed by plugs or vias having a cross section in the plane of the interlayers with dimensions that are much longer in one direction, resulting in vias with a very low aspect ratio in one dimension and with appreciably reduced foot-print in the device and compatible with design rules as applied to conducting paths in the device layers.

Fig. 2

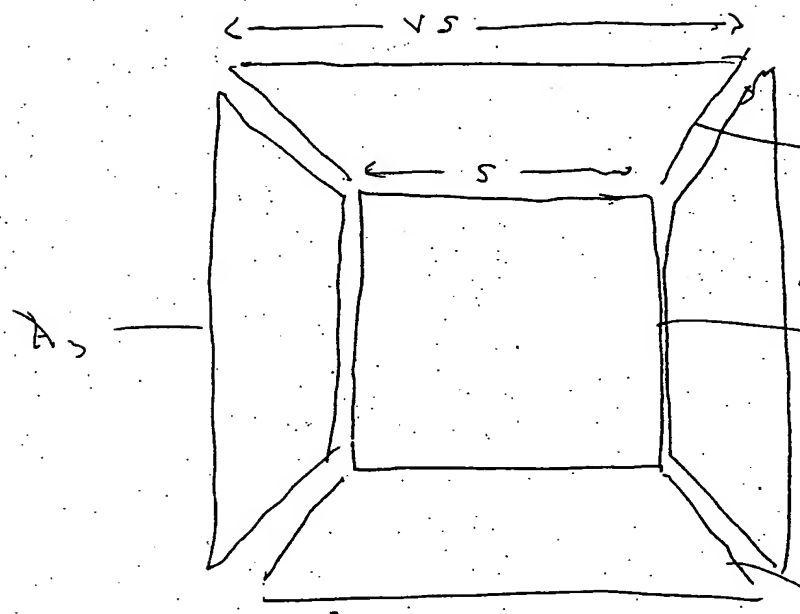


Fig 1

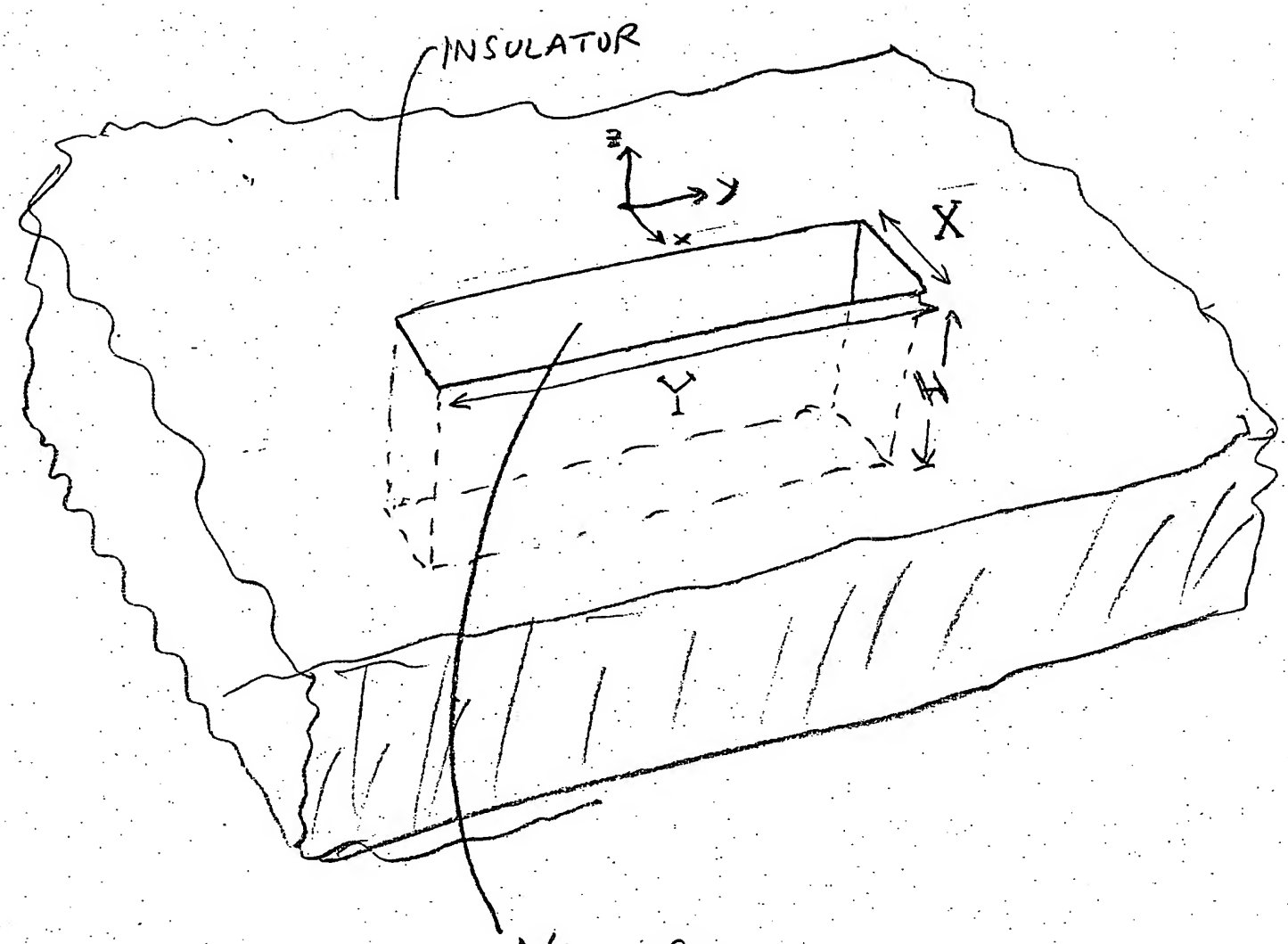
$$A_k = \frac{vs + s}{2} \cdot \frac{vs - s}{2}$$

$$A_2 = \frac{s^2(v^2 - 1)}{4}$$

$$A = \sum_{k=1}^{k=4} A_k = \frac{4s^2(v^2 - 1)}{4}$$

$$= s^2(v^2 - 1)$$

FIG. 2



VIA OPENING:

H/X → HIGH ASPECT RATIO IN x-DIRECTION

H/Y → LOW " " IN y- " "

FIG. 3

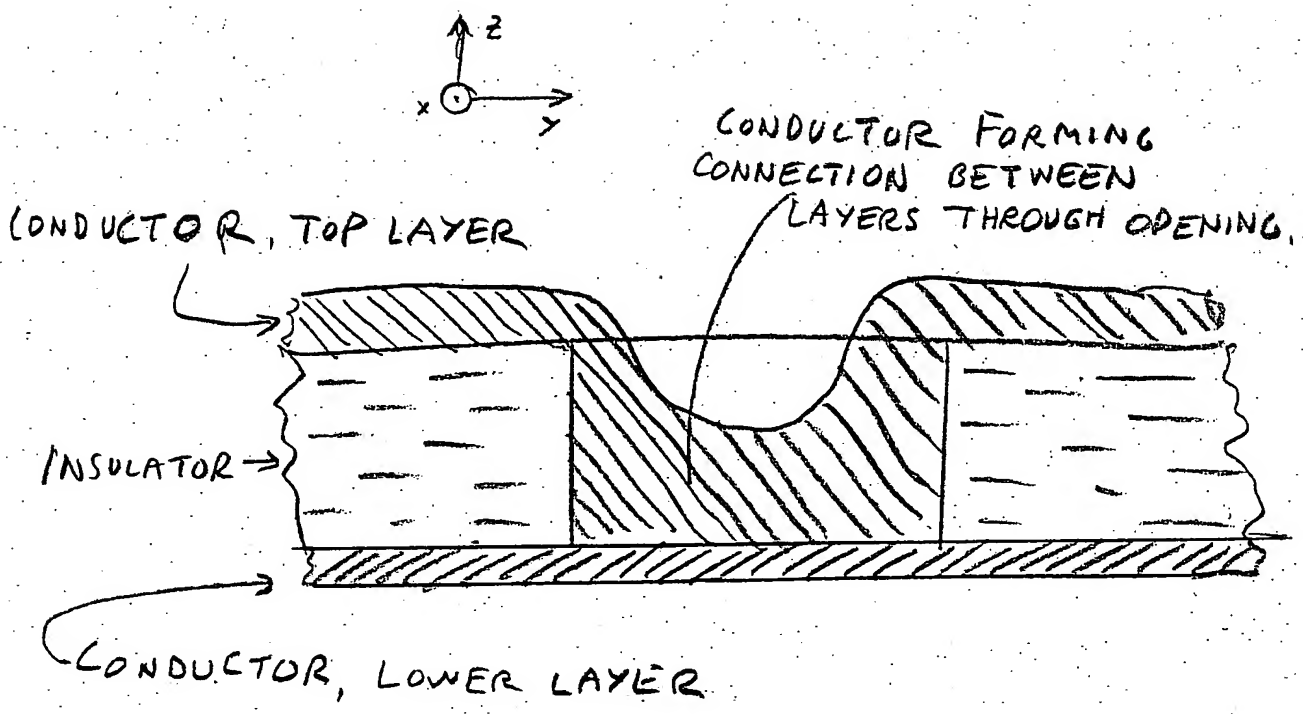


FIG 4

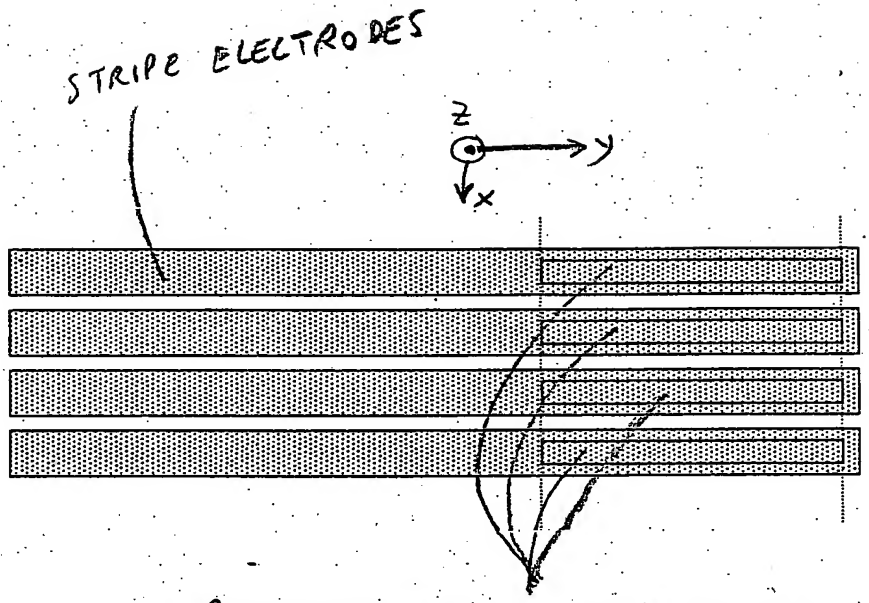


FIG 5